A HIGH GAIN, MONOLITHIC DISTRIBUTED AMPLIFIER USING CASCODE ACTIVE ELEMENTS

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ABSTRACT

A novel, monolithic, distributed amplifier has achieved a record gain of over 10 dB from 2-18 GHz. The design utilizes five quarter-micron gate length, cascode connected, FETs on epitaxial material. Circuit simulations predict over 10 dB gain from 2-30 GHz for an amplifier with seven active elements. Novel features of the design, fabrication and testing are discussed.

INTRODUCTION

By combining the benefits of cascode connected FET active elements with quarter-micron gate lengths, a novel, 12 dB gain, 2-20 GHz distributed amplifier has been designed. Over 10 dB gain from 2-18 GHz, as well as a minimum noise figure of 4 dB at 7 GHz, have been achieved on working circuits. Additional features which facilitated this gain achievement include FETs of varying gate width and fabrication on OMVPE GaAs.

Previous amplifiers of this type have been characterized by relatively low gain. R. Pauley et al. [1] have reported a 2-40 GHz amplifier with 4 dB gain; and, in fact, others have reported designs achieving about 7 dB gain in the 2-20 GHz range [2]. Advantages of a high gain distributed amplifier include a reduction in current consumption, interstage loss and gain ripple to achieve, for instance, a broadband, 20 dB gain module.

CIRCUIT DESIGN

Important gain-enhancing effects for distributed amplifiers exist by replacing the conventional, half-micron gate length, common-source FET with a quarter-micron gate length, cascode active element, as shown in Fig. 1. In particular, a careful analysis of distributed amplifiers [3] shows that gain bandwidth product is limited by loss associated with gate and drain line loading by the FETs of the circuit. We have taken the approach that only by a simultaneous reduction in both gate and drain line parasitic loss is the circuit able to accommodate appreciably more gate

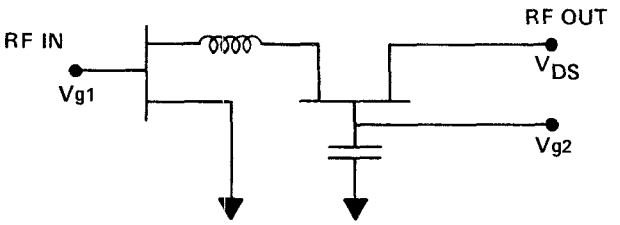

Fig. 1: Cascode active element with biasing.

periphery and obtain a higher total transductance and overall gain. Since parasitic loss mechanisms within the FET, such as source-drain output conductance, reduce both $|S_{11}|$ and $|S_{22}|$ of the active element, any reasonable method of augmenting both these parameters, without introducing a degradation of $|S_{21}|$ or stability problems, will potentially enhance the gain capability of the distributed amplifier. A remedy used to reduce gate loading and extend bandwidth is to use shorter gate length FETs [1] with their reduced gate capacitance. However, short gate length FETs can exhibit increased output conductance which can thwart significant improvements in gain. D. Dawson et al. [4] has demonstrated the use of cascode sections in a 2-6 GHz hybrid distributed amplifier using discrete 1.0 micron FETs. In this work we demonstrate the additional advantage of cascode sections for monolithic distributed amplifiers employing 0.25 micron FETs.

To mitigate loss on both gate and drain lines we have taken the unique approach of combining the synergistic benefits of quarter-micron gate length FETs in a cascode configuration. To substantiate this, near D.C., the input and output impedances for the cascode active element are

$$Z_{in} = r_i + \frac{1}{j\omega C_{gs}}, \quad r_i \approx \frac{1}{2g_m}$$

$$Z_{out} = (2 + \mu)\, r_{ds}, \quad \mu = g_m\, r_{ds} \approx 10$$

It is seen that, by employing the quarter-micron gate length, cascode active element, Z_{in} is more reactive, since C_{gs} is halved, and Z_{out} is increased by an order of magnitude. As seen in Fig. 2, a plot of $|S_{11}|$ and $|S_{22}|$, for the cascode active element, shows these benefits extend to high frequencies. A more detailed analysis shows additional benefits such as double pole peaking of $|S_{21}|$ by insertion of an inductive element between drain and source of the two FETs, which has, incidentally, been incorporated in our design.

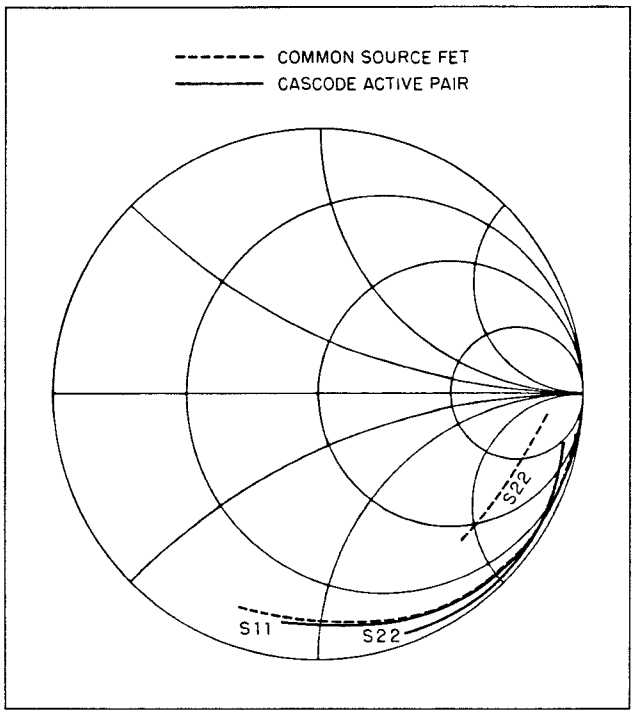

Fig. 2: $|S_{11}|$, $|S_{22}|$ for .5 μm × 150 μm common-source FET ($N_{act} = 3\times10^{17}/cm^3$) and a .25 μm×150 μm cascode active element ($N_{act} = 5\times10^{17}/cm^3$).

CIRCUIT OPTIMIZATION

Because the cascode active element is composed of a common source FET followed by a common gate FET, as shown in Fig. 1, reliable optimization of cascode, distributed amplifier, design parameters requires accurate modeling of devices in both configurations. The usual approach is to fit, via optimization algorithms, an equivalent circuit model to common source data alone; but parasitics innocuous in the common-source configuration, and thus difficult to identify quantitatively, can dominate in the common-gate configuration. For instance, parasitic source pad capacitance, essentially invisible in the common-source configuration, can have great influence in the common-gate configuration. A novel approach to FET modeling achieves this accuracy by optimizing a single FET model to fit common source, gate and drain data for a typical quarter-micron device. This new procedure results in a highly accurate FET model that can be utilized in any configuration. Results of this modeling are shown in Fig. 3.

Calculation of the cascode, distributed amplifier, design parameters required CAD optimization of twenty-four, independent parameters, including twelve gate, drain line lengths and five FET widths. In order to ensure that a global optimum was achieved with such a prohibitive number of independent parameters, the optimization was carried out in successive stages in which increasing numbers of parameters were admitted to the optimization process.

An extremely useful feature of our FET model allows for continuous variation of gate width during optimization. We have found this added degree of freedom to improve return loss, gain flatness and overall gain by 1-2 dB, in much the same way that adjusting internal elements of a lumped filter tunes its performance.

Results of the optimization indicate that 12 dB ± .1 dB gain from 2-20 GHz is achievable for a distributed amplifier with five cascode active elements. Another design with seven active elements should achieve over 10 dB of gain from 2-30 GHz.

FABRICATION

A photo micrograph of the completed distributed amplifier is shown in Fig. 4. The overall chip size is 1.8 mm by 3.0 mm. Clearly visible are the cascode active elements of varying gate width, gate and drain lines of varying length and on chip terminations.

To the best knowledge of the authors, this circuit is the first report of a MMIC to be fabricated on organometallic vapor phase epitaxial (OMVPE) GaAs. It should be noted that discrete FETs fabricated on OMVPE and MBE GaAs showed little or no difference in performance. A distinct advantage we found in using epi-material, as opposed to ion-implanted material, is the lack of FET g_m compression. Thus circuit performance is relatively insensitive to the gate recess etch depth. In applications which require low current consumption or noise figure, I_{dss} can be tailored to a reduced value. It should be noted that the high gain result, presented in this paper, had an associated I_{dss} of only 150 mA.

Other key features of the fabrication process include mesa isolation, mesa resistors, metal-insulator-metal (MIM) capacitators, airbridges and backside vias. Quarter-micron gates, of over 90% yield, were fabricated by exposing PMMA with a computer controlled SEM capable of step and repeat exposing as well as automatic alignment and focusing. Alignment marks on individual FETs are still visible, as seen in Fig. 4. Gate yield was markedly improved after it was discovered that tweezer damage to the PMMA during processing caused particulate obscuration of the gate opening during

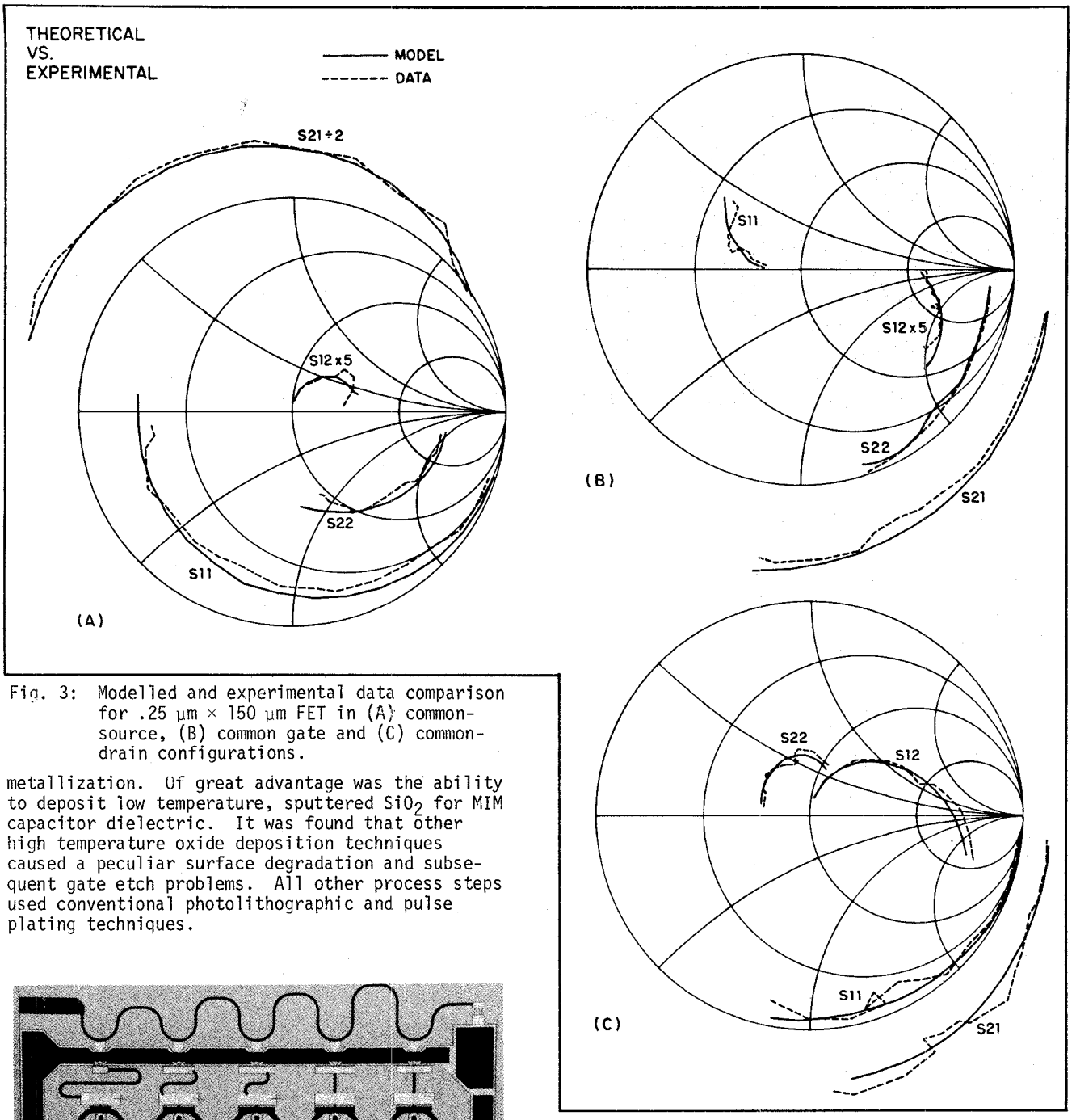

Fig. 3: Modelled and experimental data comparison for .25 μm × 150 μm FET in (A) common-source, (B) common gate and (C) common-drain configurations.

metallization. Of great advantage was the ability to deposit low temperature, sputtered SiO_2 for MIM capacitor dielectric. It was found that other high temperature oxide deposition techniques caused a peculiar surface degradation and subsequent gate etch problems. All other process steps used conventional photolithographic and pulse plating techniques.

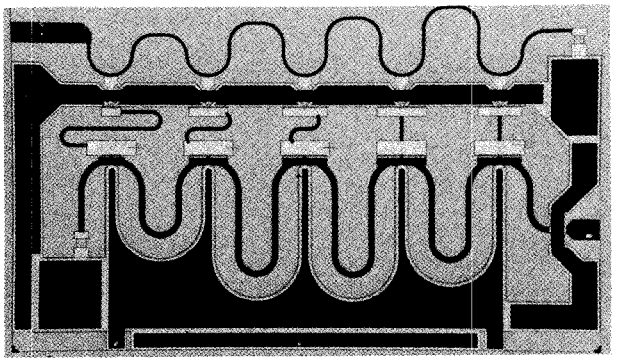

Fig. 4: Photo micrograph of cascode distributed amplifier. Chip size .18 mm × .30 mm.

TESTING AND RESULTS

Biasing of the cascode, distributed amplifier is identical to the common-source FET amplifier except that an additional bias on the gate of the common gate FET, as shown in Fig. 1, is required. By varying this additional bias, the gain of the circuit is adjustable, thus providing an added feature of automatic gain control. A D.C. measurement of an amplifier is displayed in Fig. 5 yielding a total gm of 250 mmhos for 940 microns

of gate periphery and an extremely low output conductance which is characteristic of the cascode configuration.

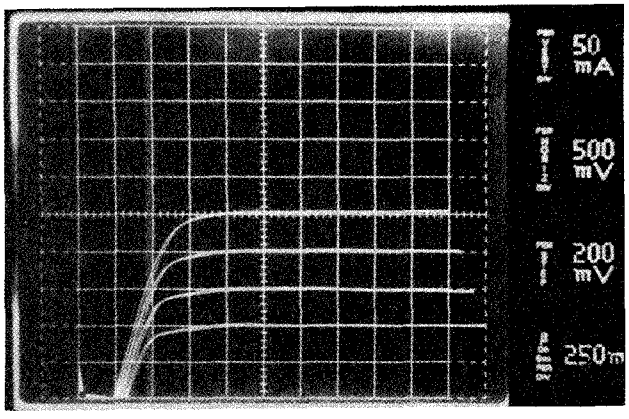

Fig. 5: D.C. durve tracer measurement showing I_{ds} - V_{ds} curve for amplifier.

R.F. measurements from 2-20 GHz were taken using an R.F. wafer probe station; Fig. 6 displays results of over 10 dB from 2-18 GHz. This is the highest reported gain for a single stage distributed amplifier. Return loss is greater than 10 dB throughout the band. The two high gain regions are confirmed by computer modeling to be due to high termination resistors, 80 Ω, at the low end and poor gate R.F. grounding of the common gate FET at the high end. Poor R.F. grounding leads to oscillations at the band edge. Computer modeling indicates that these two problems can be overcome by reduction of termination resistance to 50 Ω and incorporation of improved backside vias for good R.F. grounding; with these improvements flat gain response of 12 dB ± .25 dB is achievable. Both corrections have been incorporated in circuits under fabrication at the time of this writing.

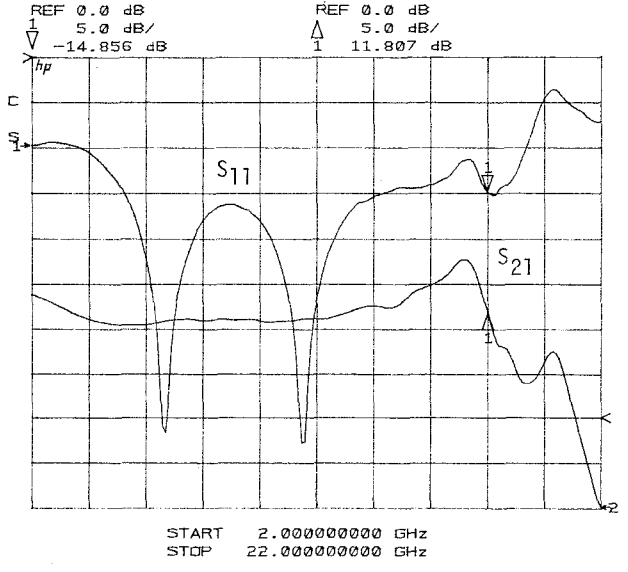

Fig. 6: Gain and return loss measurements. V_{ds} = 5.0 V, V_{g1} = -.20 V, V_{g2} = +.72 V, I_{ds} = 150 mA.

Noise figure and associated gain were measured from 4-15 GHZ by using the same R.F. wafer probe station, and these results, displayed in Fig. 7, record a noise figure of 4 dB and associated gain of over 10 dB at 7 GHz. The low value of I_{dss} is responsible for simultaneous high gain and low noise figure. It must be emphasized that the lower noise figures are attributable to the use of quarter-micron gate lengths and not to the cascode configuration [4], [5].

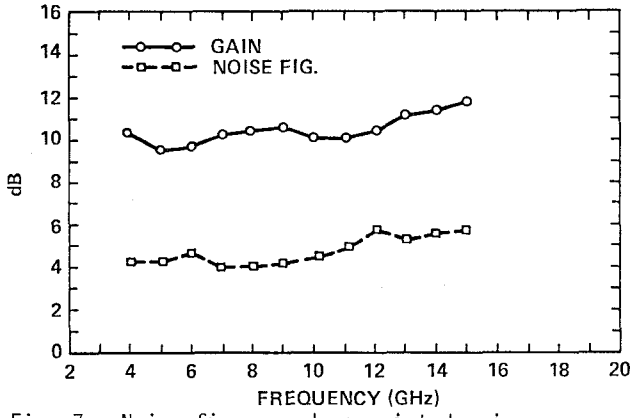

Fig. 7: Noise figure and associated gain measurements. V_{ds} = 4.0 V, V_{g1} = -.55 V, V_{g2} = +1.50 V, I_{ds} = 93 mA.

CONCLUSION

The results presented in this paper demonstrate that single-stage, monolithic, distributed amplifiers can be fabricated with over 10 dB gain from 2-18 GHz and amplifiers with 12 dB flat gain from 2-20 GHz are achievable. It has been shown that the combination of quarter-micron gate lengths and the cascode configuration can improve both the gain and noise figure. Careful modeling of the active elements in all configurations is key to the design. While gain flatness, on working circuits, was afflicted with R.F. grounding problems, computer modeling indicates flat gain response of 12 dB from 2-20 GHz once this problem is resolved.

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